# Towards Detection and Monitoring of Ageing Precursors on the XFEL Machine Beam Control Hardware

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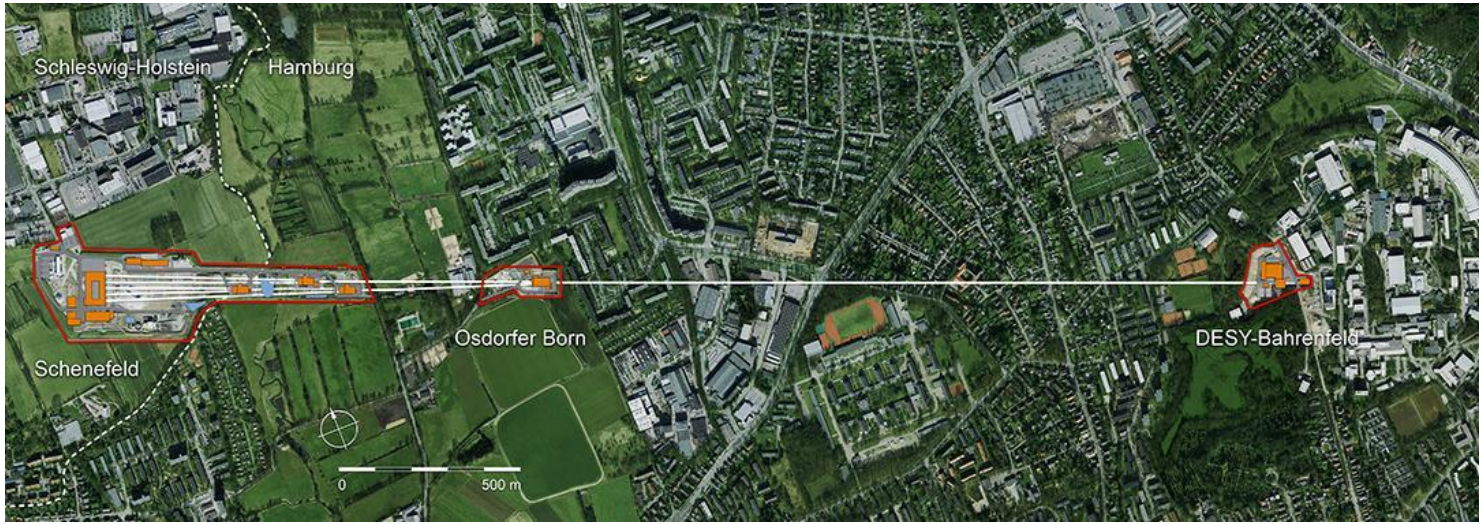
# European X-Ray Free-Electron Laser (XFEL)

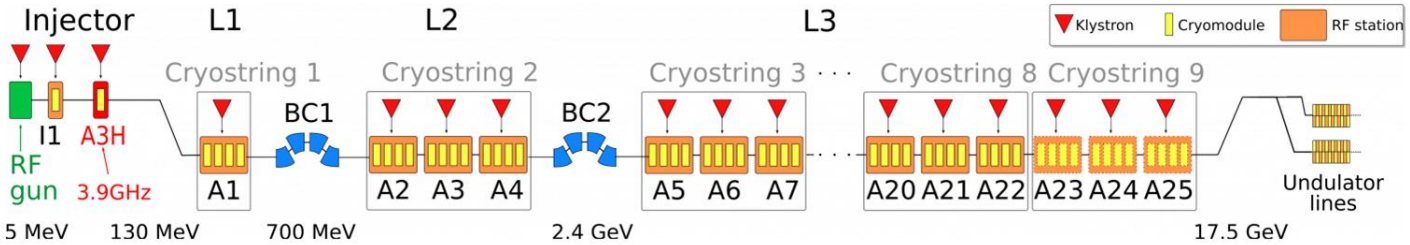



- Longest superconducting linear accelerator in the world (3.4 Km)
  - 768 Niobium RF cavities over 1.7 Km
  - Maximum energy delivery of 17.4 GeV

**Image: https://xfel.desy.de/**

# European X-Ray Free-Electron Laser (XFEL)

## Machine Beam Control (MSK) Group




**MSK Primary Operation Sub-Groups**

Figure: Julien Branlard

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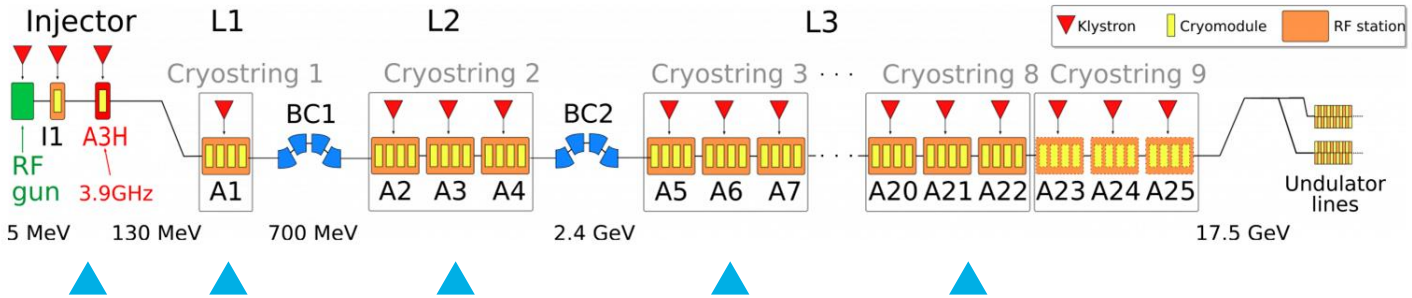


**MSK Primary Operation Sub-Groups**

**Low-Level RF Control**

Figure: Julien Branlard

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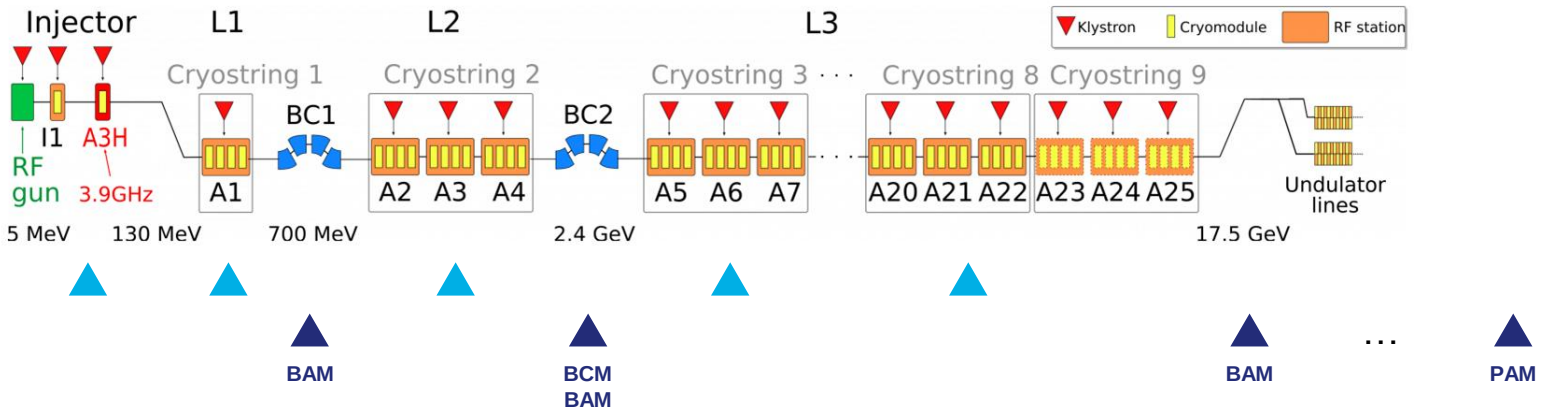


**MSK Primary Operation Sub-Groups**

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**Special Diagnostics**

Figure: Julien Branlard

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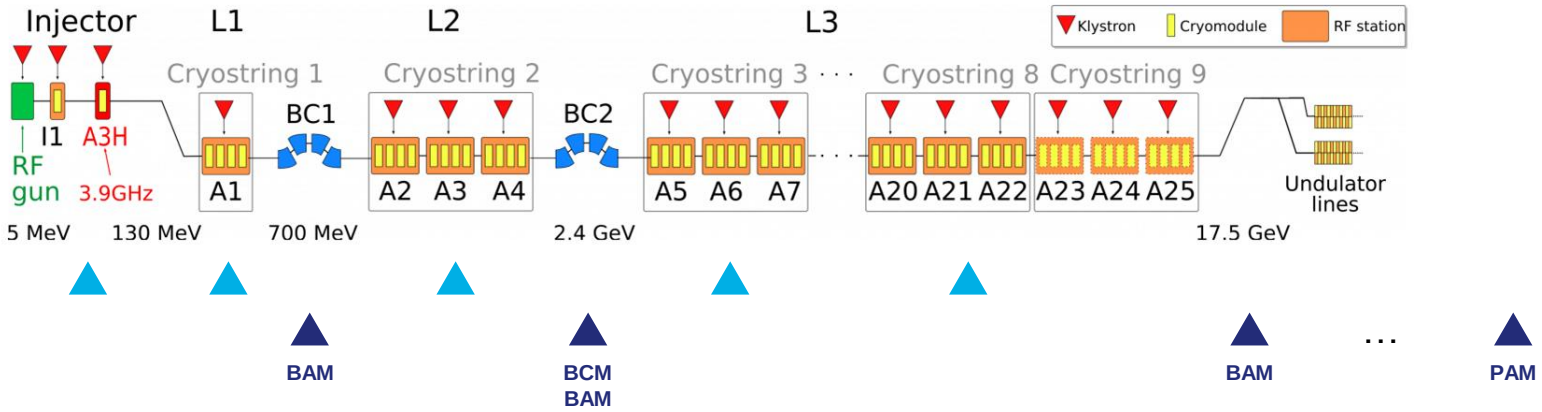


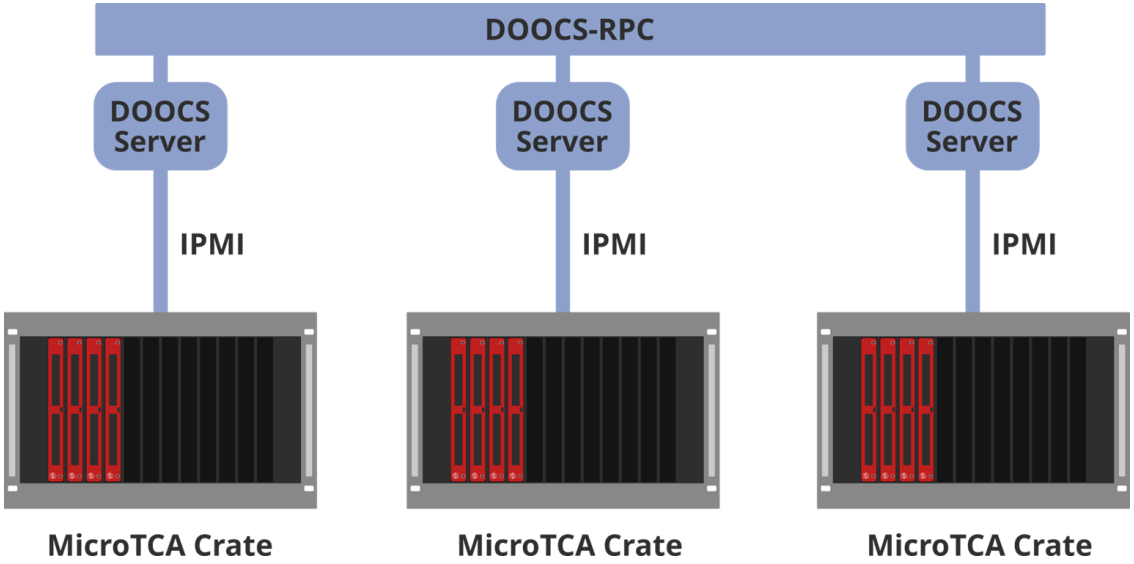

**MSK Primary Operation Sub-Groups**

- Low-Level RF Control
- Special Diagnostics
- Optical Synchronization

Figure: Julien Branlard

# European X-Ray Free-Electron Laser (XFEL)

## MSK Group Hardware



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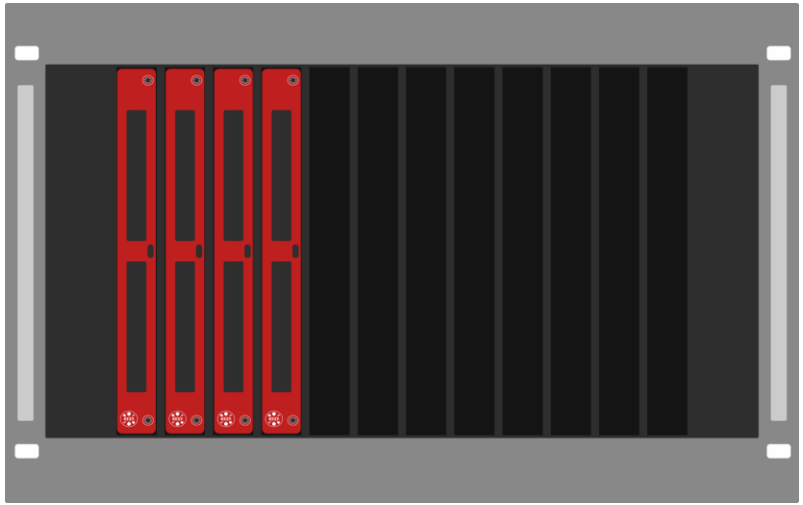

**MicroTCA Crate**

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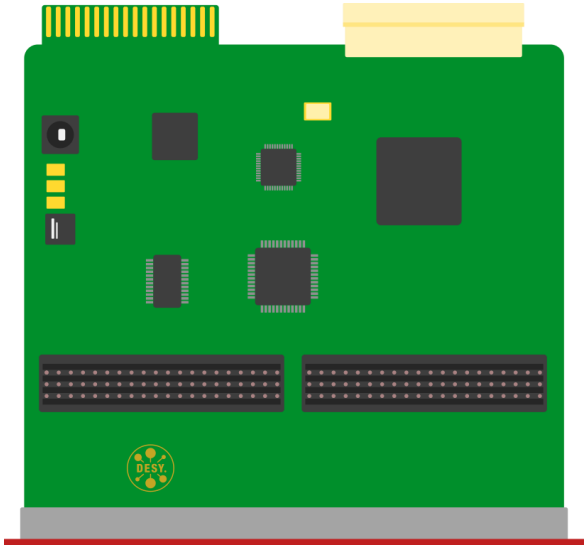


**DAMC-FMC20 Carrier Board**

# European X-Ray Free-Electron Laser (XFEL)

## MSK Group Hardware

**FMC20**
Carrier Board

**FMC25**
Carrier Board

**TCK7**
Data Processing and Telecommunication Board

**and more…**

Images: MicroTCA Technology Lab

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- **High dependability**

Images: MicroTCA Technology Lab

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  *“Ability to perform as and when required.”*

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  **Reliability, Availability, Maintainability…**

Images: MicroTCA Technology Lab

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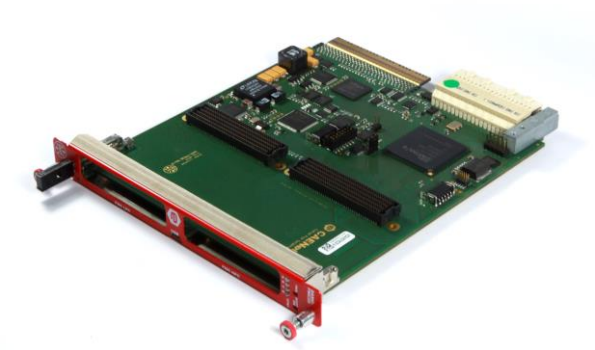

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**and more…**

- **High dependability**
- **Long-term operation**
  - **Thermal Cycles**
  - **Enhanced Radiation**

Images: MicroTCA Technology Lab

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⇒ **Hardware Ageing**

Images: MicroTCA Technology Lab

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Images: MicroTCA Technology Lab

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⇨ **Hardware Ageing** ⇨ **Ageing Precursors** ⇨ **Failures**

Images: MicroTCA Technology Lab

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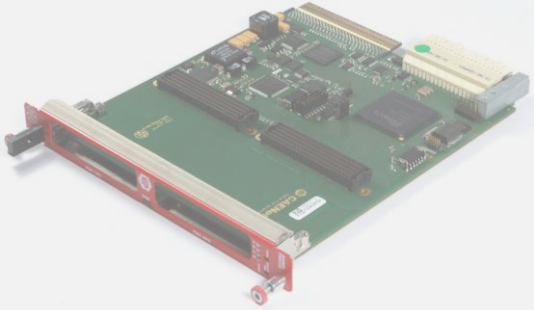

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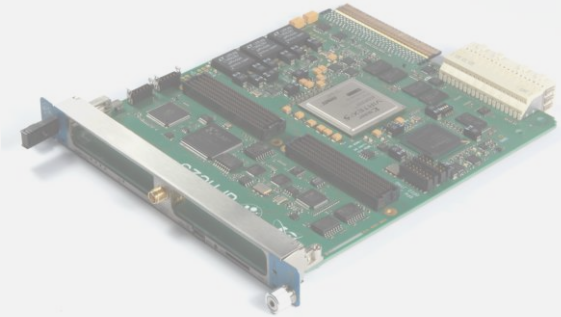

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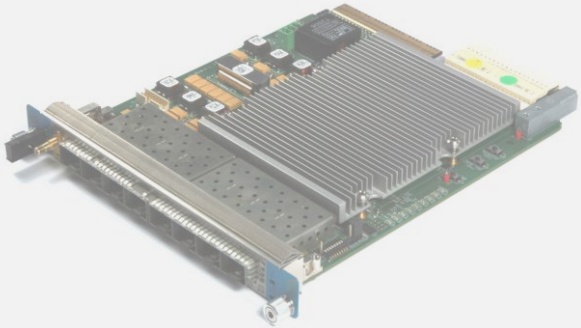


**TCK7**
Data Processing and Telecommunication Board

and more…

- High dependability
- **Long-term operation**
  - **Thermal Cycles**
  - **Enhanced Radiation**

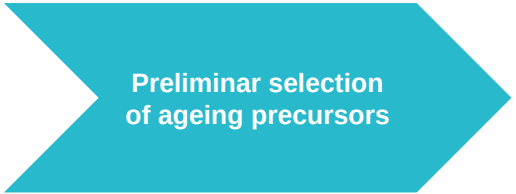
Images: MicroTCA Technology Lab

**Monitor**

Hardware Ageing ⇒ **Ageing Precursors** ⇒ Failures

- **To estimate remaining useful life**
- **To perform predictive maintenance**

# Project Plan
## Find Relevant Features



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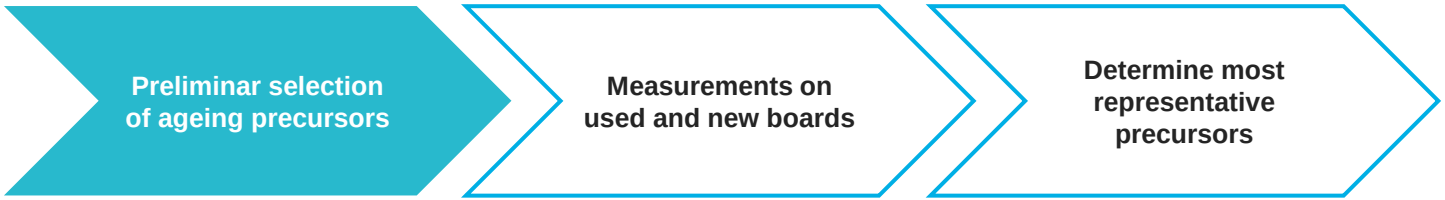

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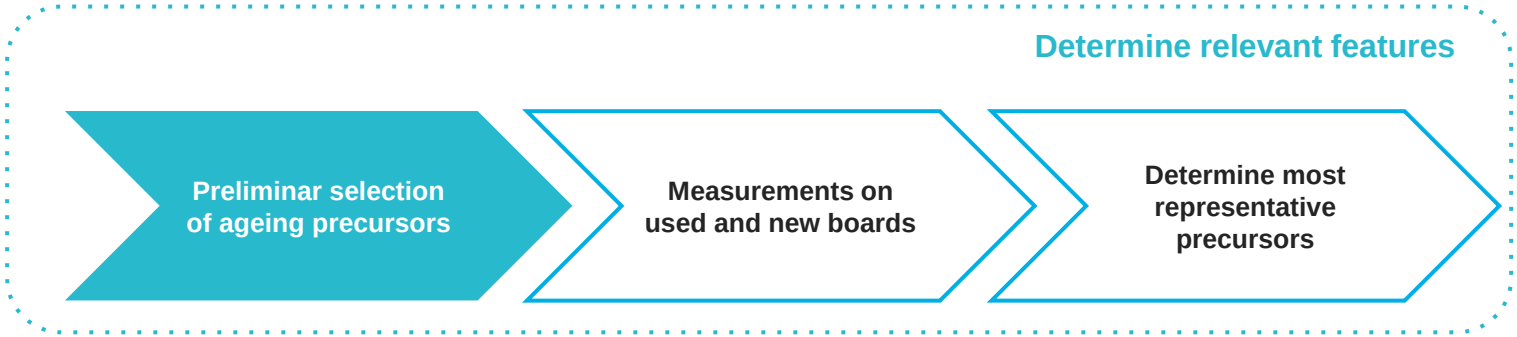

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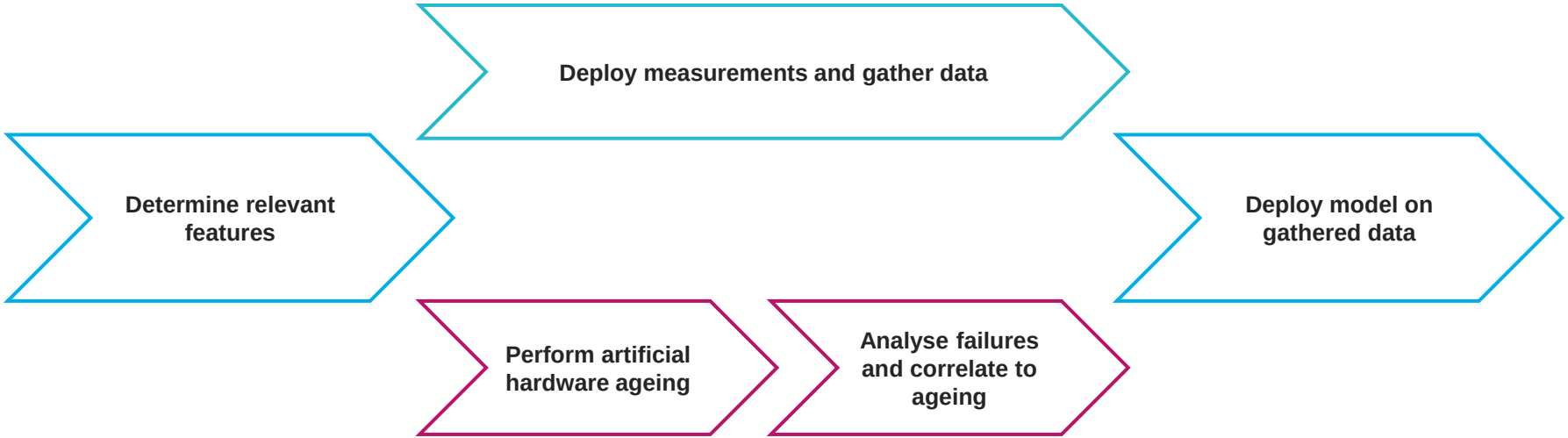

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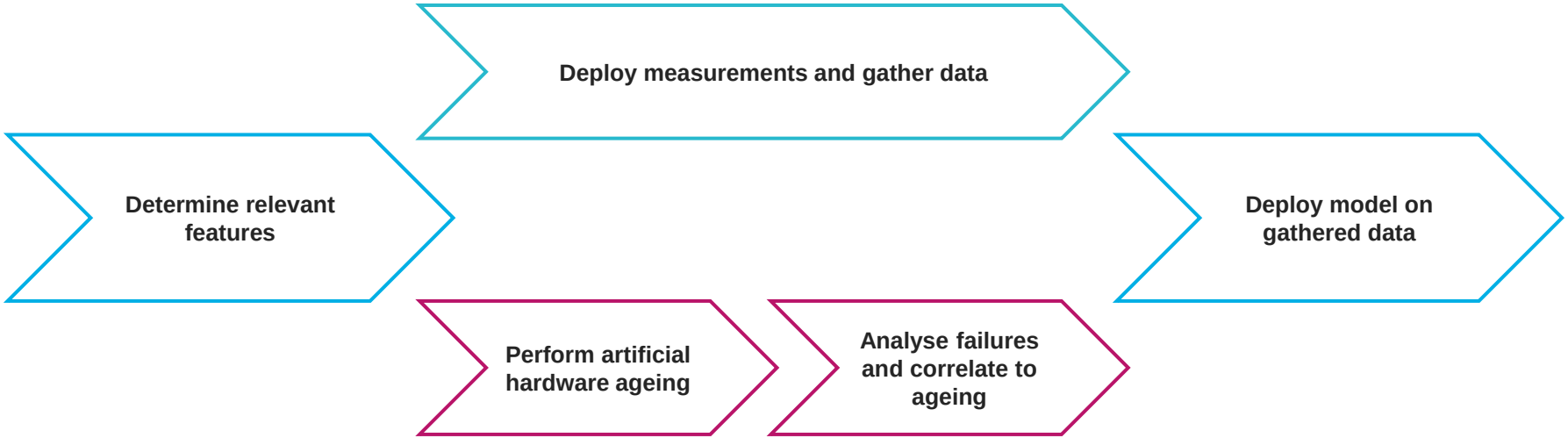

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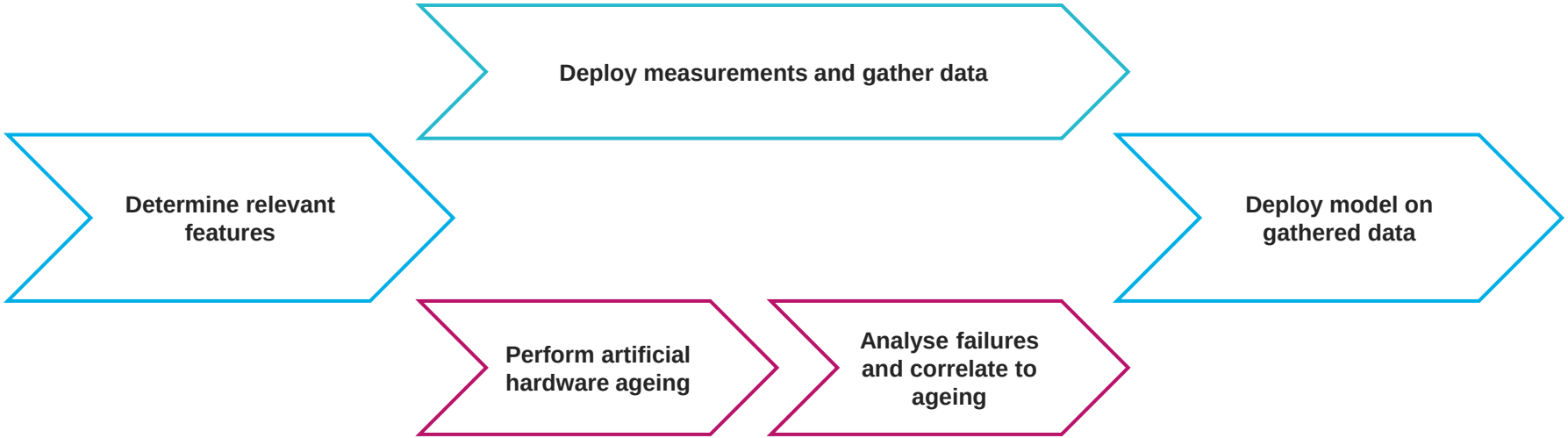
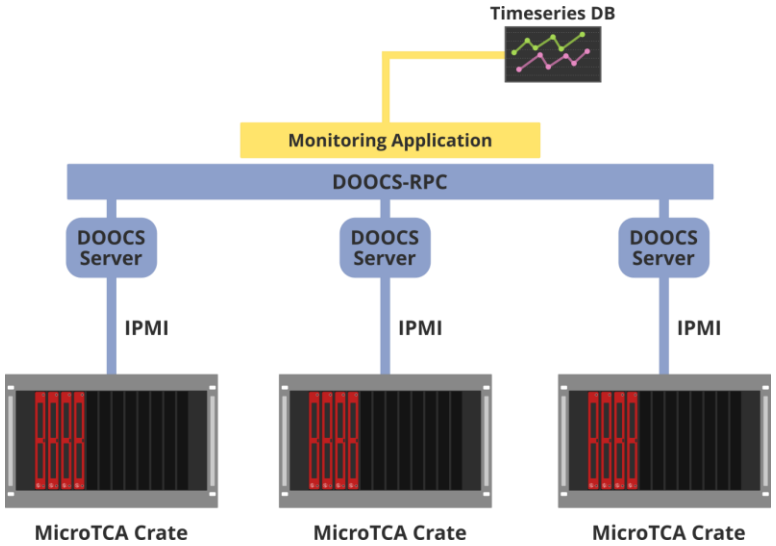



Problem Understanding | Relevant Data Gathering | Data Cleaning & Analysis | Model Development | Model Deployment

# Ageing Precursors Monitoring
## Overview & Challenges




- **Devices**
  - Perform self-tests
  - Expose parameters on DOOCS
- **Monitoring application**
  - Collects measurements of exposed parameters
  - Stores data in a time series DB for analysis
- **Challenges**
  - Select representative ageing precursors
  - Self-tests without hardware alterations
  - No interference with running applications

# Potentially Affected Components

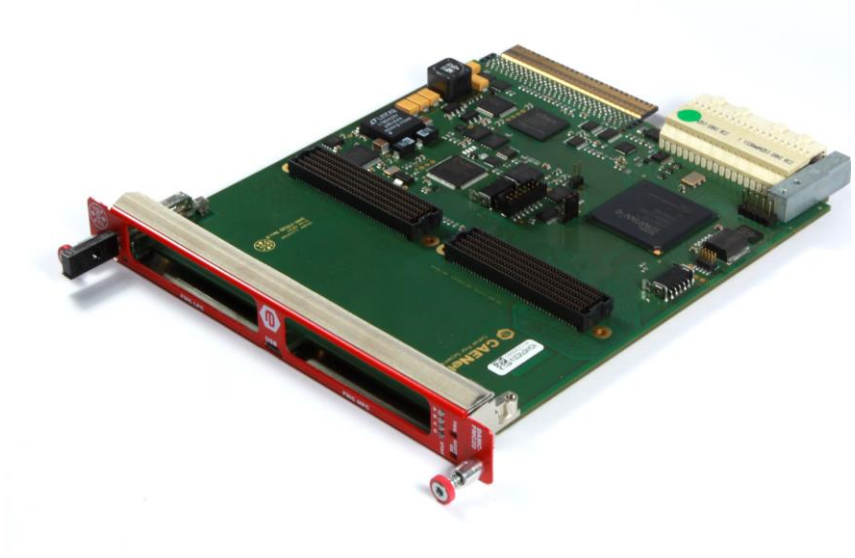


Image: MicroTCA Technology Lab

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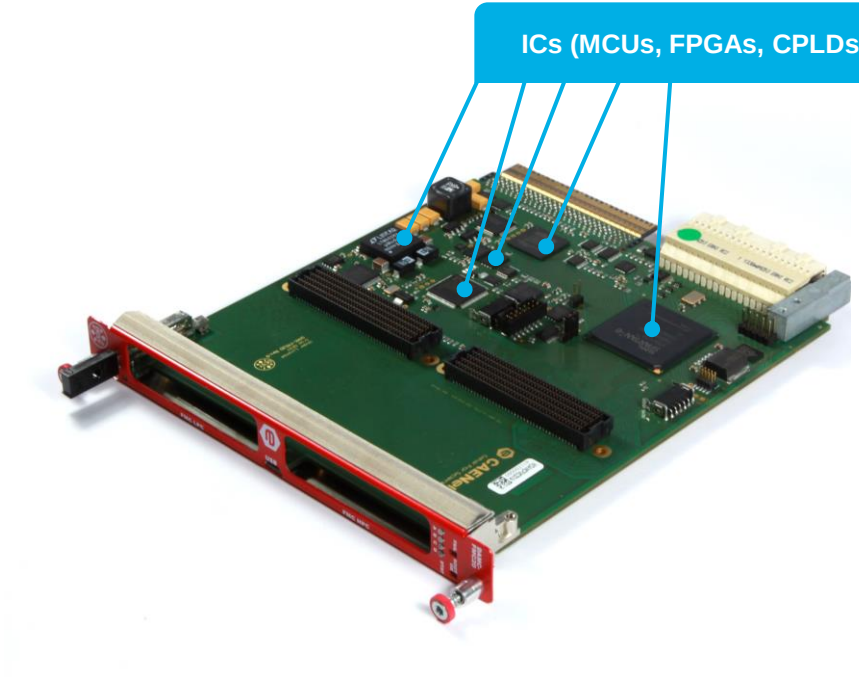


- Modifications in critical paths
- Timing issues
- Degradation and reduced bandwidth of high-speed links

Image: MicroTCA Technology Lab

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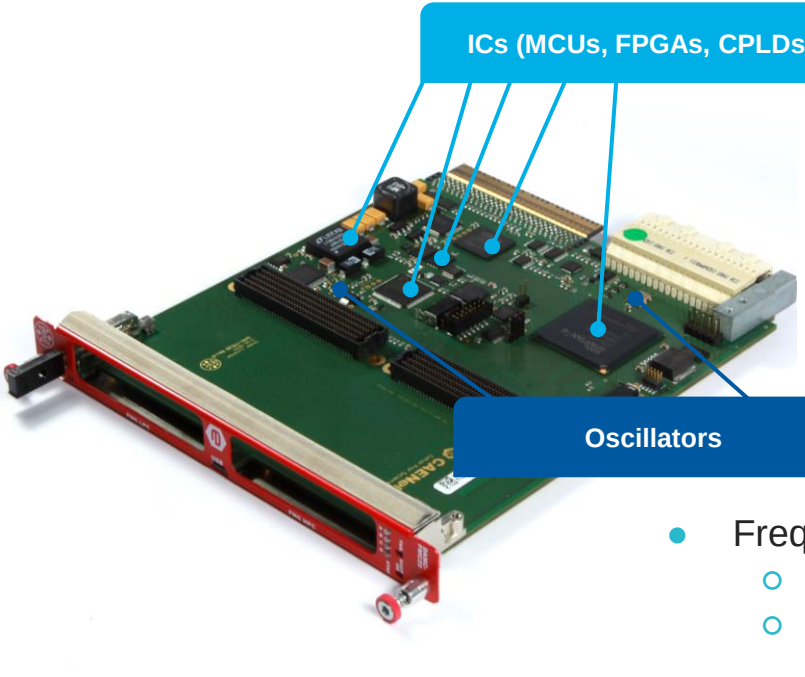


- Modifications in critical paths
- Timing issues
- Degradation and reduced bandwidth of high-speed links

- Frequency shifting
  - Crystal oscillators
  - RC oscillators

Image: MicroTCA Technology Lab

# Ageing Mechanisms

- Semiconductors
- Interconnects
- Crystals

# Ageing Mechanisms

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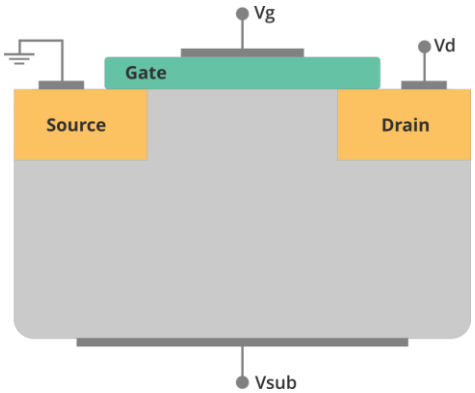
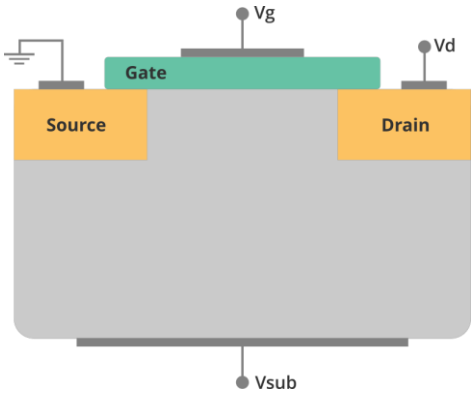
# Ageing Mechanisms
## Semiconductors




- The Metal-Oxide-Semiconductor Field-Effect Transistor (**MOSFET**) is the building-block of today's electronics
- Widely used as an electrical switch in digital electronics

# Ageing Mechanisms
## Semiconductors

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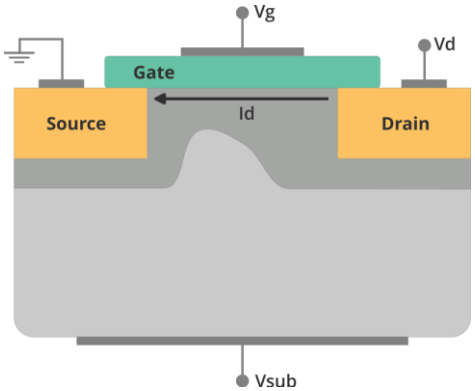


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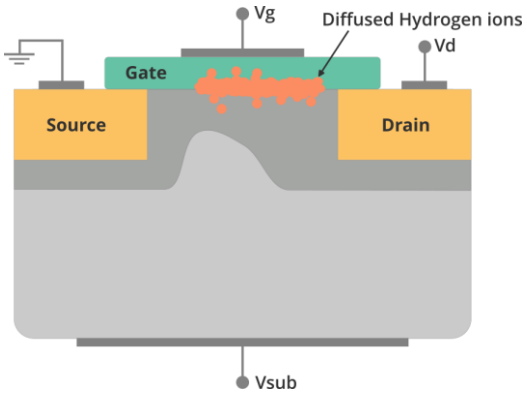
- Widely used as an electrical switch in digital electronics
- When a voltage is applied only to the Drain ($V_d$), no current passes
- When, in addition, a voltage on the Gate ($V_g$) greater than a **threshold $V_{th}$** is applied, a channel forms allowing a current to flow.

# Ageing Mechanisms

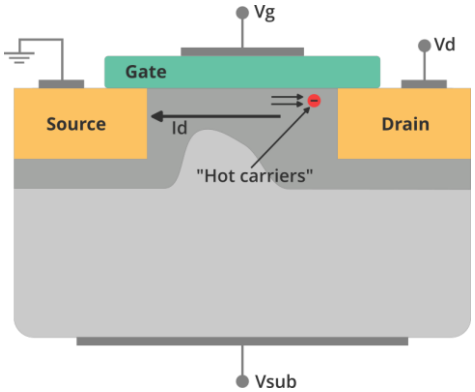
## Semiconductors - Negative Bias Temperature Instability (NBTI)




- Static mechanism affecting p-MOSFETs due to interface traps
  - **Increased** $V_{th}$
  - **Reduced** drain current
  - **Slower switching speed**
- Partial recovery exists => degradation depends on **duty cycle**

# Ageing Mechanisms

## Semiconductors - Hot Carrier Injection (HCI)



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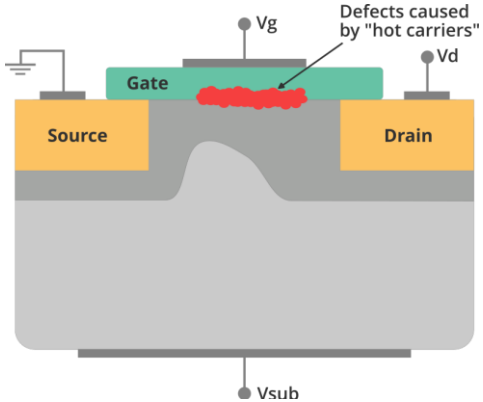
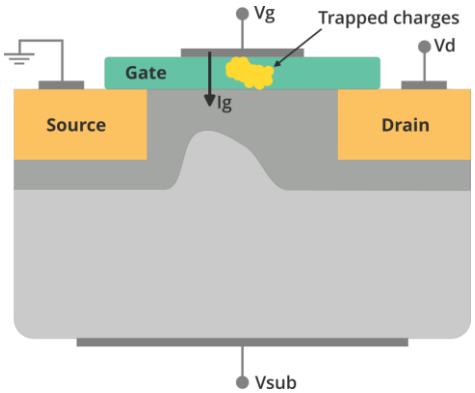



- Dynamic mechanism at high $V_d$
  - **Increased** $V_{th}$
  - **Slower switching speed**
- Has no recovery mechanism => degradation depends on **switching activity**

# Ageing Mechanisms

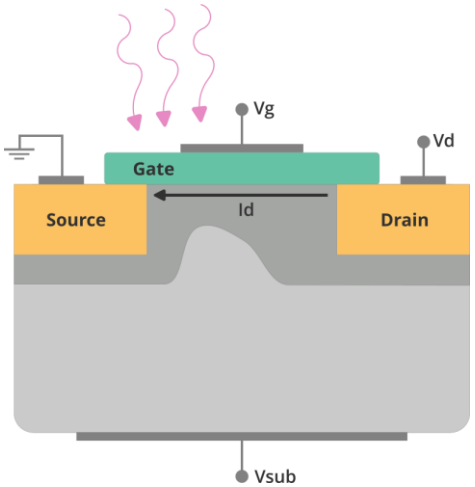
## Semiconductors - Time-Dependent Dielectric Breakdown (TDDB)




- Static mechanism due to oxide defects
  - **Increased** gate leakage current ($I_g$)
  - **Slower switching speed**
- Has no recovery mechanism

# Ageing Mechanisms

## Semiconductors - Radiation-Induced Trapped Charges



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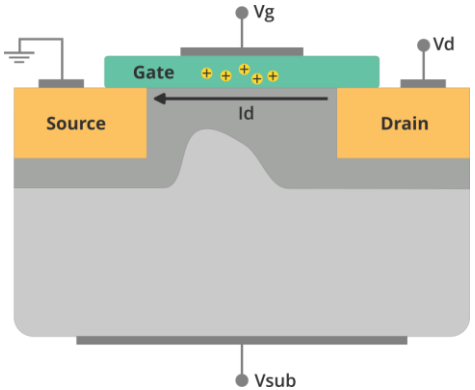


- Ionizing radiation causes positive charges to be trapped in the oxide
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- Has a slow recovery mechanism (from seconds to years)

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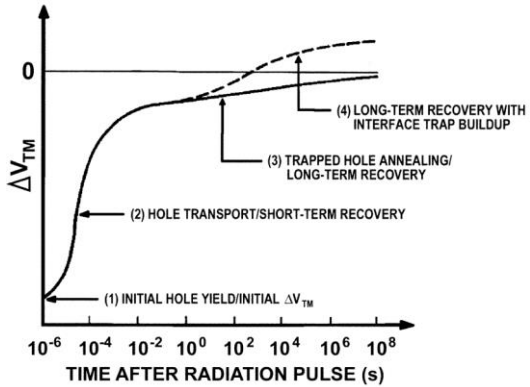


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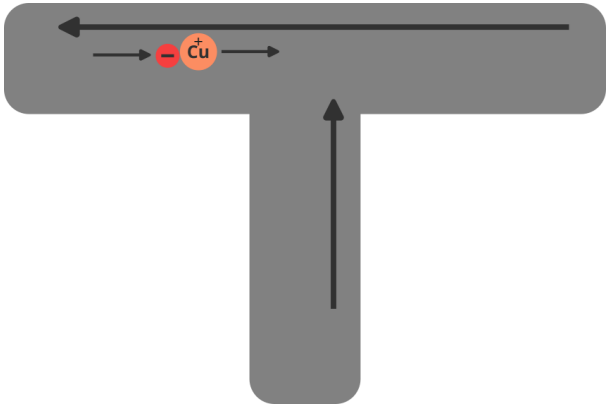
T. R. Oldham and F. B. McLean, "Total ionizing dose effects in MOS oxides and devices," in IEEE Transactions on Nuclear Science, vol. 50, no. 3, pp. 483-499, June 2003
doi: 10.1109/TNS.2003.812927.

# Ageing Mechanisms

- Semiconductors
- **Interconnects**
- Crystals

# Ageing Mechanisms

## Interconnects - Electro Migration (EM)




- Ions **migrate** due to **high current density**
  - **Increased** impedance
  - **Slower switching**
  - **Open / Short** circuits
- Has no recovery mechanism

# Ageing Mechanisms

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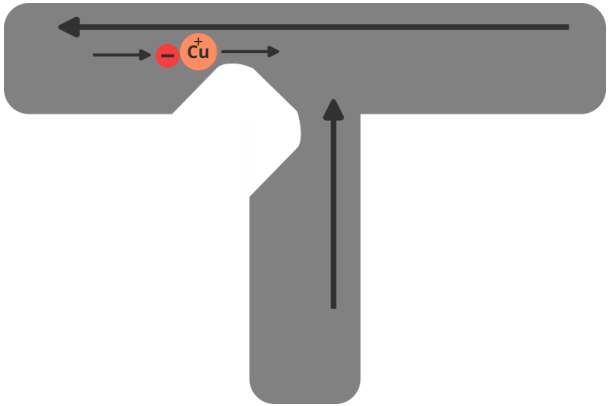


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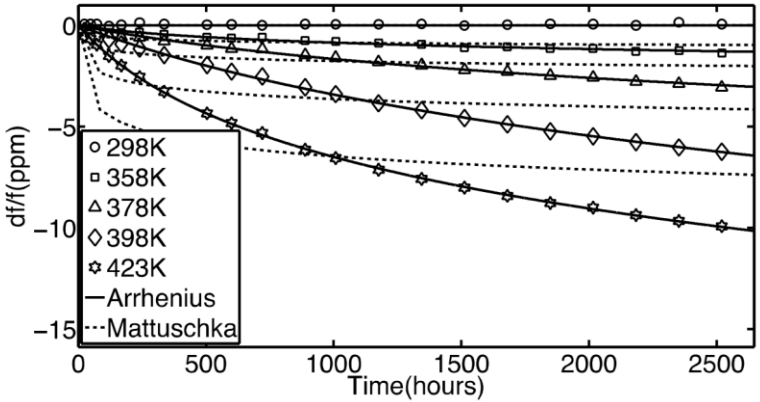
# Ageing Mechanisms
## Quartz Crystals




- **Frequency shifting** due to
  - **Mass transfer** due to contamination
  - **Stress relief** (mounts, bonds, etc.)
  - **Radiation**
  - Quartz **degassing**

S. -y. Wang et al., "Aging models and parameters of quartz crystal resonators and oscillators," 2015 Symposium on Piezoelectricity, Acoustic Waves, and Device Applications (SPAWDA), 2015, pp. 382-385, doi: 10.1109/SPAWDA.2015.7364512.

# Sensing Ageing Effects

- Field Programmable Gate Array (FPGA)
- Microcontroller
- Static RAM (SRAM)
- Low Drop-Out Voltage Regulator
- Oscillator

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- **Field Programmable Gate Array (FPGA)**
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# Sensing Ageing Effects

## FPGA Propagation Delay Measurement

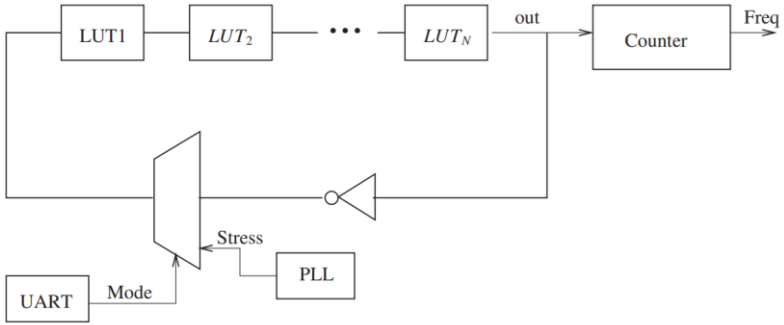


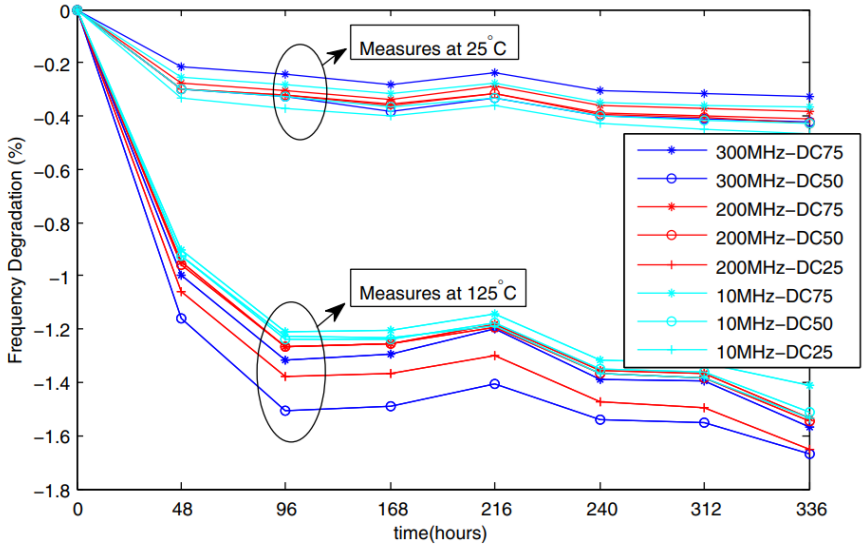

**Fig. 1.** RO-based sensor structure.

- Ring-Oscillator (RO) sensor circuit
  - Odd number of inverters
  - Frequency **proportional** to propagation delay (switching speed)
  - Artificially aged by a stress signal
- Tests conditions
  - Different temperatures
  - Varying stress signals
  - Multiple RO architectures


M. Slimani et al.,"Analysis of ageing effects on ARTIX7 XILINX FPGA", Microelectronics Reliability,Volumes 76–77, 2017, pp. 168-173, doi: 10.1016/j.microrel.2017.07.006

# Sensing Ageing Effects

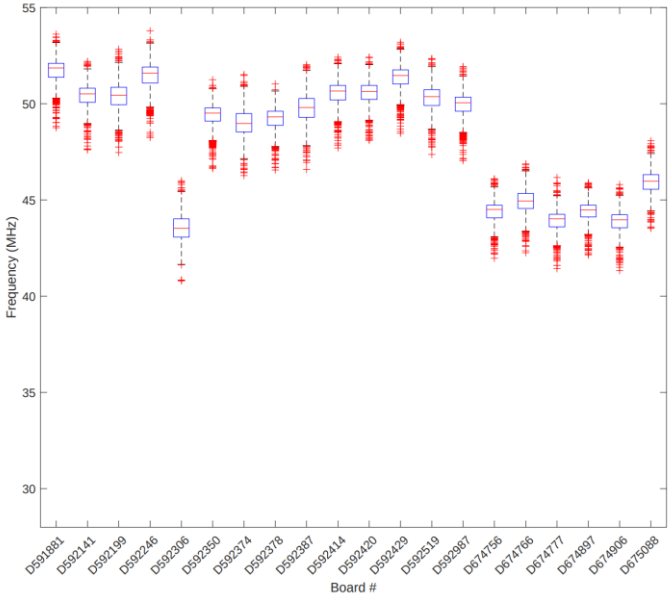
## FPGA Propagation Delay Impact




- Highly dependent on stress signal duty cycle
- More degradation at higher temperature and frequency (due to recovery)
- **Average frequency degradation of 1.7%**


M. Slimani et al.,"Analysis of ageing effects on ARTIX7 XILINX FPGA", Microelectronics Reliability,Volumes 76–77, 2017, pp. 168-173, doi: 10.1016/j.microrel.2017.07.006

# Sensing Ageing Effects
## FPGA Propagation Delay Mapping




- Instantiation of multiple RO sensor circuits over the FPGA fabric at the same time
- Evaluation on multiple aged devices

P. Cheng, “Study of Monitoring Circuitry for Ageing in FPGAs”, Master Thesis, 2021, Department of Electrical and Information Technology, Lund University, Sweden

# Sensing Ageing Effects
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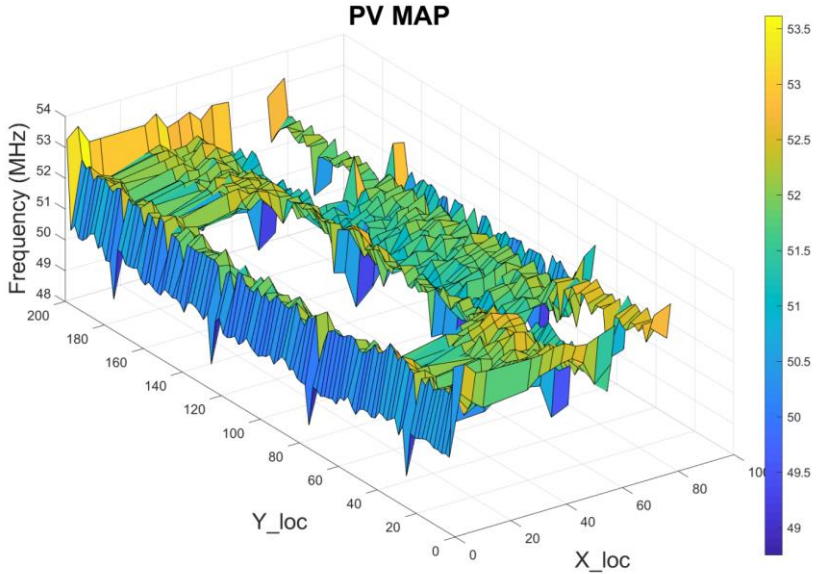


- Using placement information, a frequency degradation map can be created, by measuring individual ROs

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# Sensing Ageing Effects

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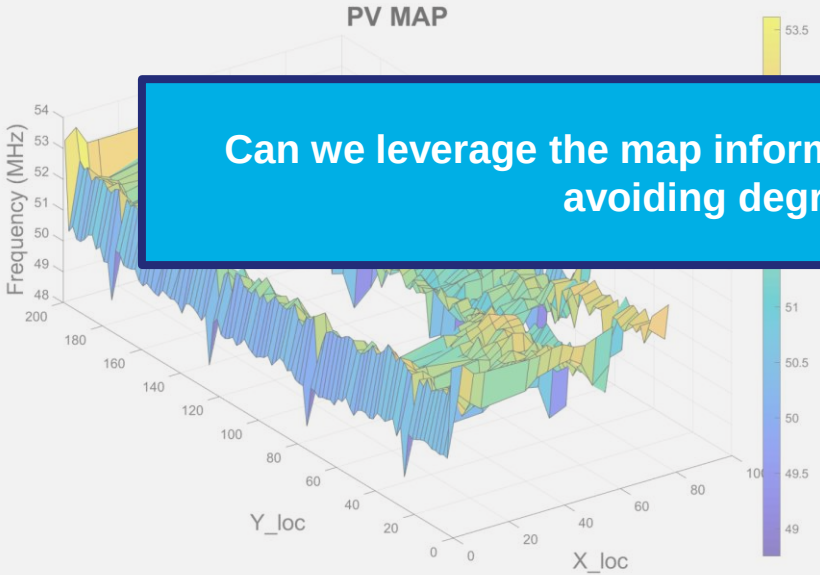


**Can we leverage the map information to constrain the place & route, avoiding degraded FPGA areas?**

e
created, by measuring individual ROs

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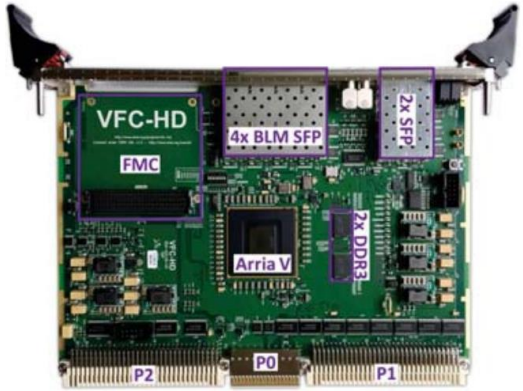
# Sensing Ageing Effects

## FPGA Optical Links Transceiver Degradation




- Test and validation strategy for the new Large Hadron Collider (LHC) Beam Loss Monitor (BLM) processing module
- Optical link transceivers appeared as the weak point
  - Highly affected by operating temperature, due to degradation

V. Schramm et al., "Combined Testing And Validation Strategy For The New LHC BLM Processing Module"
2019 Annual Reliability and Maintainability Symposium (RAMS), 2019, pp. 1-7,
DOI: 10.1109/RAMS.2019.8769268.

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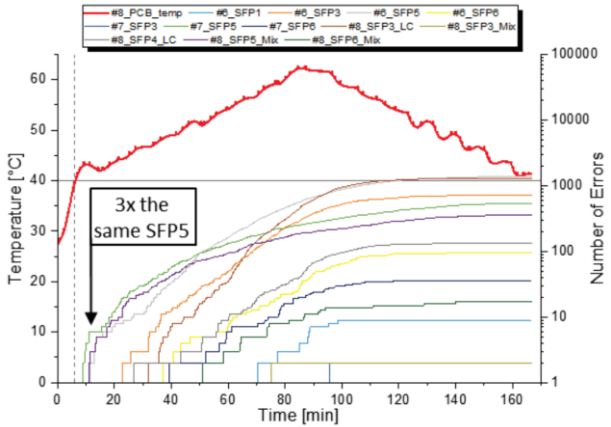


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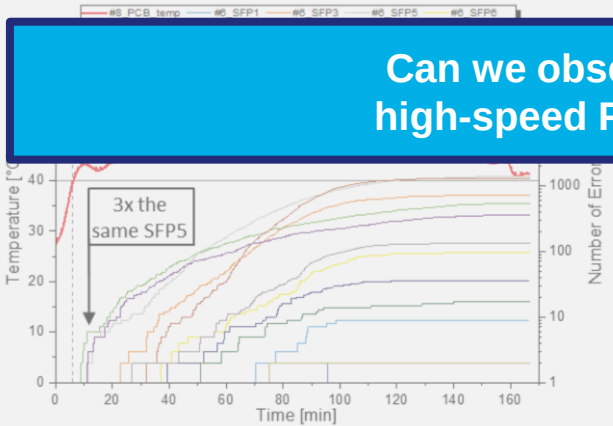


**Can we observe a degradation on the high-speed FPGA links due to ageing?**

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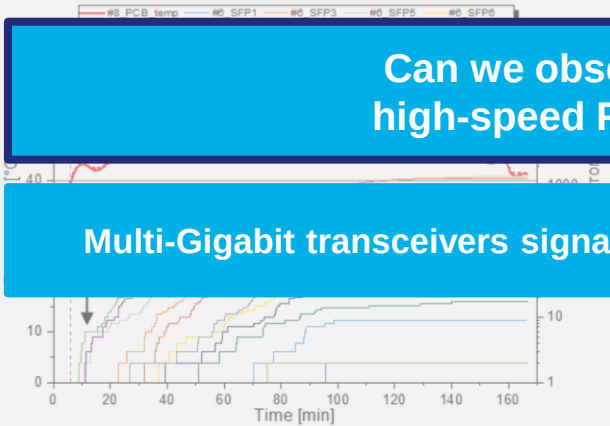


**Can we observe a degradation on the high-speed FPGA links due to ageing?**

**Multi-Gigabit transceivers signals**

**Maximum DDR RAM bandwidth**

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V. Schramm et al., "Combined Testing And Validation Strategy For The New LHC BLM Processing Module" 2019 Annual Reliability and Maintainability Symposium (RAMS), 2019, pp. 1-7, DOI: 10.1109/RAMS.2019.8769268.

# Sensing Ageing Effects

- Field Programmable Gate Array (FPGA)
- **Microcontroller**
- Static RAM (SRAM)
- Low Drop-Out Voltage Regulator
- Oscillator

# Sensing Ageing Effects

## MCU Switching Speed

**Can we detect degraded switching speed on the MCU?**

- To account for hardware ageing, vendors define bandgaps for safe operation during the guaranteed lifetime
- At lower supply voltages, the increased $V_{th}$ may affect functionality if the clock frequency is not reduced accordingly

# Sensing Ageing Effects
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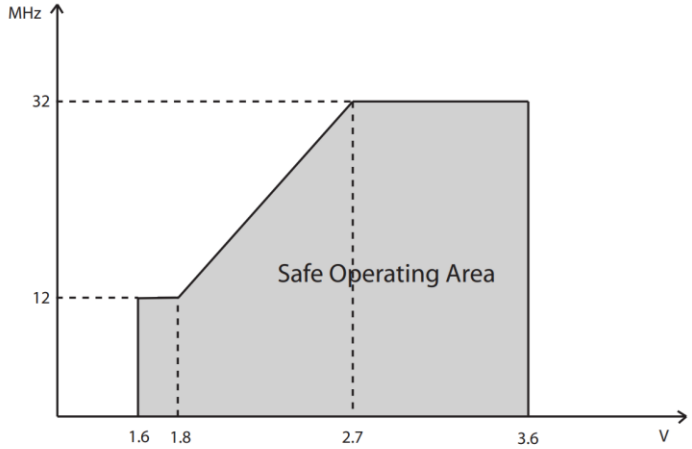


**Maximum Frequency vs. $V_{CC}$**

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Figure: Microchip ATxmega128A1U Data Sheet

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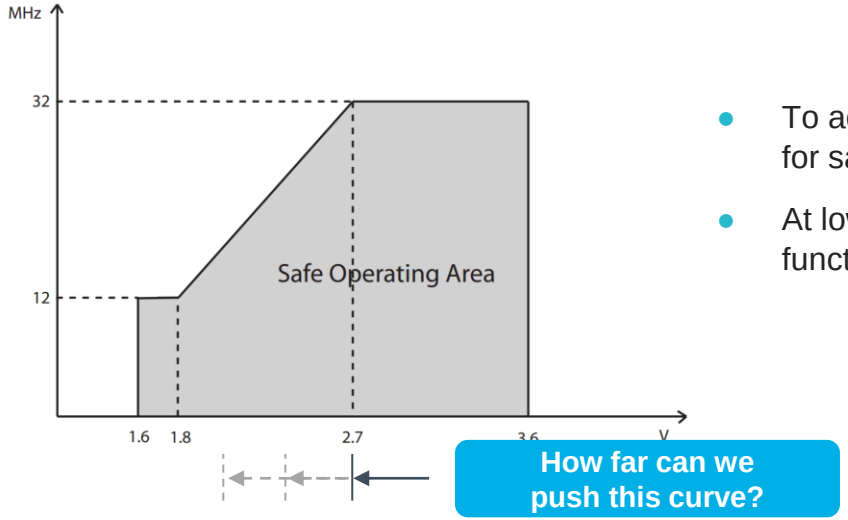


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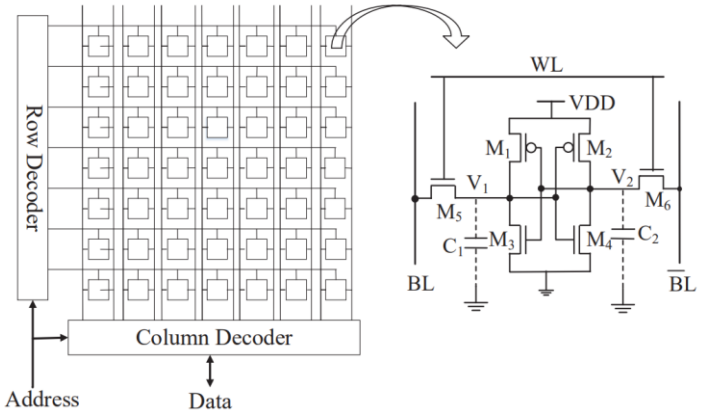
# Sensing Ageing Effects

- Field Programmable Gate Array (FPGA)
- Microcontroller
- **Static RAM (SRAM)**
- Low Drop-Out Voltage Regulator
- Oscillator

# Sensing Ageing Effects
## SRAM Startup Pattern




(a) A typical SRAM array. (b) A six-transistor SRAM cell.

- Due to mostly balanced cells, SRAM startup value has ~50% of 1s (only affected by random fabrication process defects)
- Ageing additionally introduces a variation of $V_{th}$
  - Small $V_{th}$ difference => initial values are approximately random
  - Big $V_{th}$ difference => initial values are biased


U. Guin et al., "Detecting Recycled SoCs by Exploiting Aging Induced Biases in Memory Cells" 2019 IEEE International Symposium on Hardware Oriented Security and Trust (HOST), pp. 72-80, doi: 10.1109/HST.2019.8741032.

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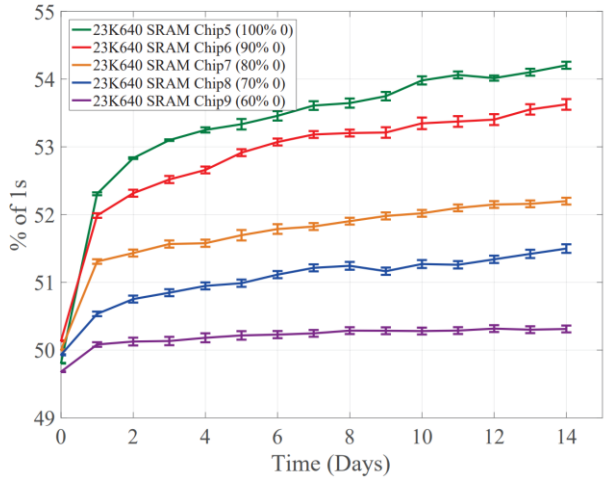


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- After continuous stress **up to 4%** more of initial 1s


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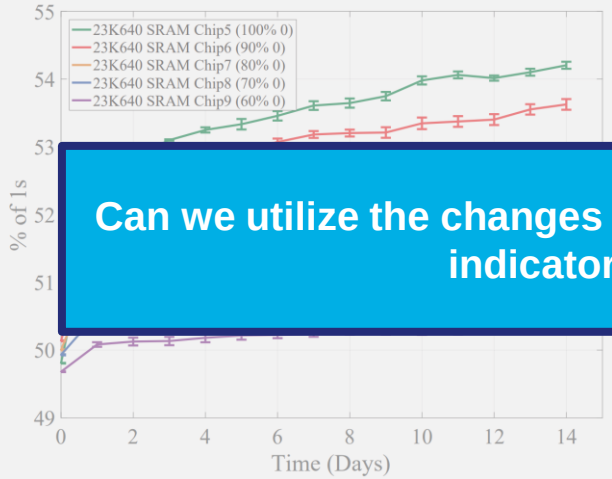


- Due to mostly balanced cells, SRAM startup value has ~50% of 1s (only affected by random fabrication process defects)

**Can we utilize the changes of the SRAM startup pattern distribution as an indicator of MCU and FPGA ageing?**

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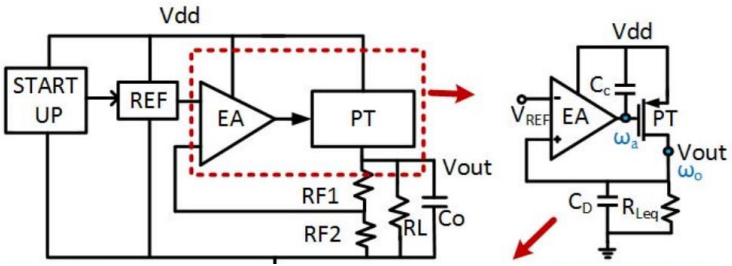
# Sensing Ageing Effects

- Field Programmable Gate Array (FPGA)
- Microcontroller
- Static RAM (SRAM)
- **Low Drop-Out Voltage Regulator**
- Oscillator

# Sensing Ageing Effects
## Low drop-out (LDO) Regulators




- LDO regulators provide a constant voltage and protect from $V_{dd}$ noise
- The Power Supply Rejection Ratio (PSRR) is the capability to suppress voltage ripples:

$$PSRR = 20 \log \left( \frac{v_{out}}{v_{in}} \right)$$

S. Chowdhury et al., "Aging Analysis of Low Dropout Regulator for Universal Recycled IC Detection" 2019 IEEE Computer Society Annual Symposium on VLSI (ISVLSI), pp. 604-609, doi: 10.1109/ISVLSI.2019.00113.

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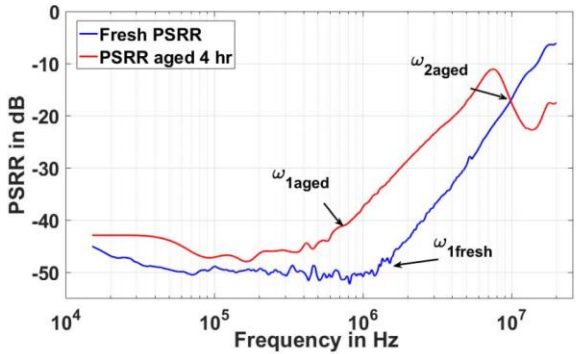


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- PSRR is affected by ageing
  - $V_{th}$ increment
  - $I_D$ decrement
  - Changes in capacitance and transconductance

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# Sensing Ageing Effects

## Low drop-out (LDO) Regulators


- LDO regulators provide a constant voltage and protect from $V_{dd}$ noise
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**Can we utilize the output ripple of the on-board LDOs to detect ageing effects?**

- PSRR is affected by ageing
  - $V_{th}$ increment
  - $I_D$ decrement
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# Sensing Ageing Effects

## On-Chip LDO Regulators

**Can we detect PSRR degradation on the On-Chip LDO regulators?**

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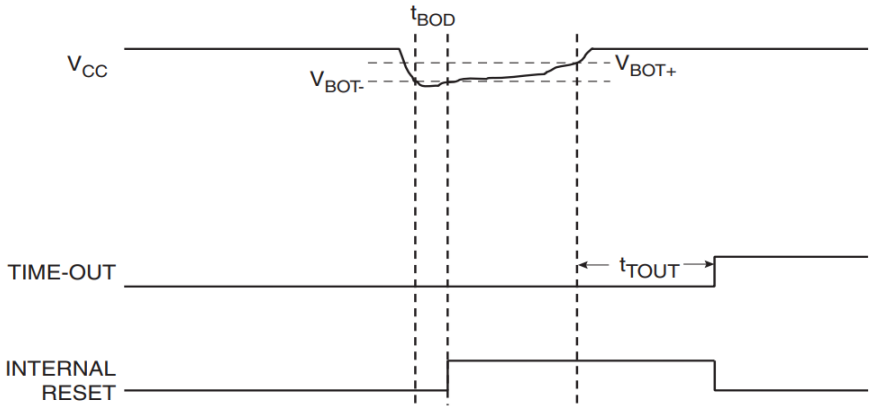


**Brownout Detection Reset**

Figure: Microchip XMEGA AU Manual

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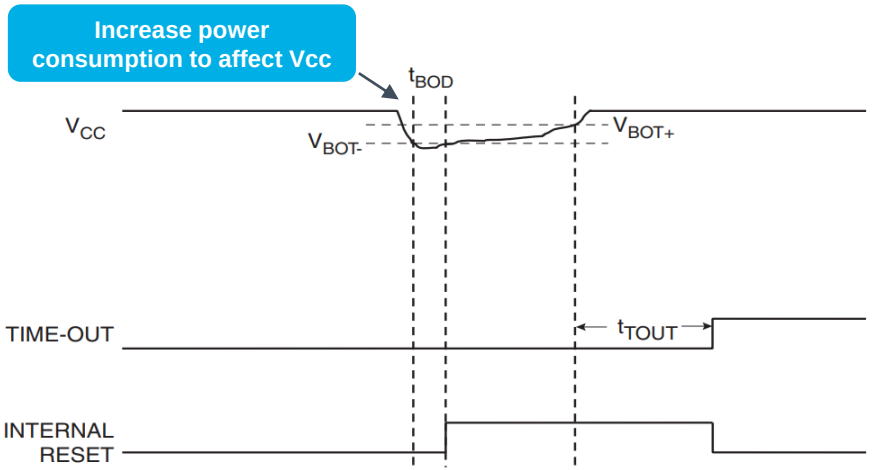


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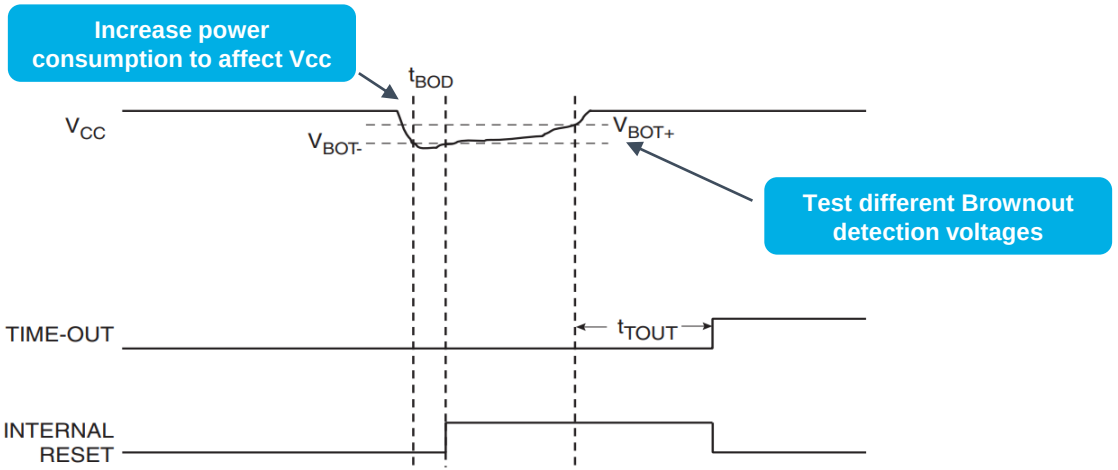


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Figure: Microchip XMEGA AU Manual

# Sensing Ageing Effects

- Field Programmable Gate Array (FPGA)
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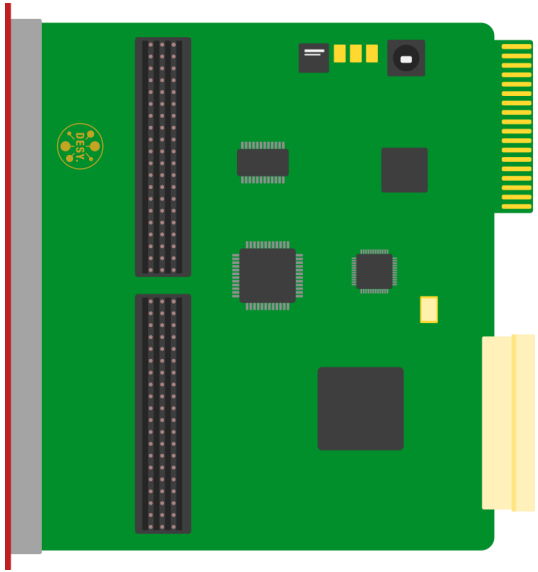
- **Oscillator**

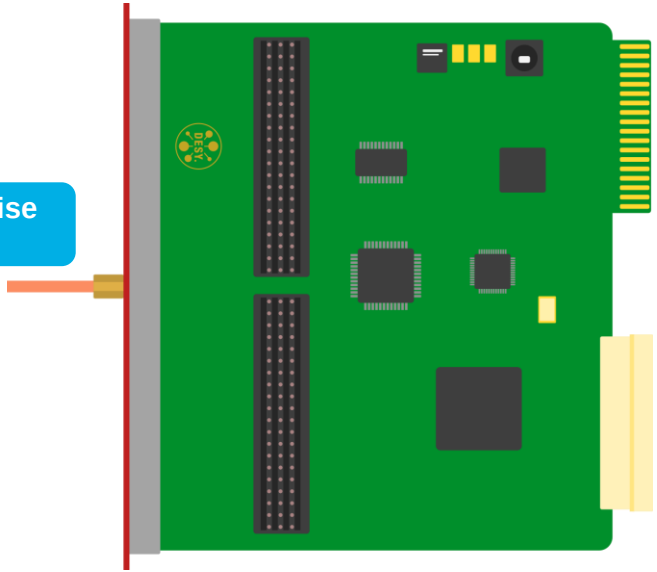
# Sensing Ageing Effects

## Oscillators Frequency Shift



# Sensing Ageing Effects

## Oscillators Frequency Shift




- Connect the external precise clock signal
- Compare crystal and internal oscillators to the known reference

# Summary

- Multiple **ageing mechanisms** come into play:
  - **Silicon**: NBTI, HCI, TDDB, radiation
  - **Interconnects**: EM
  - **Crystals**: Stress relief, mass transfer, radiation

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  - **Silicon**: NBTI, HCI, TDDB, radiation
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- We plan on **assessing the overall ageing** status via:
  - Propagation delay with ring oscillators
  - High-speed links
    - Maximum FPGA-DDR bandwidth
    - Quality of FPGA MGT signals
  - Sensitivity against low voltage at high frequencies
  - Distribution of SRAM startup pattern
  - LDO regulators PSRR (external, on-chip)
  - Oscillators frequency shift (crystal and RC)

# Thank you

Leandro Lanzieri
Deutsches Elektronen-Synchrotron

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